PROGRAMMABLE JUNCTION FIELD EFFECT TRANSISTOR AND METHOD FOR PROGRAMMING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of and claims the benefit of copending U.S. patent application Ser. No. 10/335,403, entitled "Programmable Junction Field Effect Transistor and Method for Programming Same," by Lin et al. and filed on Dec. 30, 2002 now U.S. Pat. No. 7,075,132, which is incorporated herein by reference.

FIELD OF THE INVENTION

Embodiments of the present invention relate to the field of semiconductor devices. In particular, embodiments of the present invention relate to junction field effect transistors (JFETs).

BACKGROUND ART

Junction field effect transistors (JFETs) are majority carrier devices that conduct current through a channel that is controlled by the application of a voltage to a p-n junction. JFETs may be constructed as p-channel or n-channel and may be operated as enhancement mode devices or depletion mode devices.

The most common JFET type is the depletion mode type. The depletion mode device is a "normally on" device that is turned off by reverse biasing the p-n junction so that pinch-off occurs in the conduction channel. P-channel depletion mode devices are turned off by the application of a positive voltage between the gate and source (positive V_{gs}), whereas n-channel depletion mode devices are turned off by the application of a negative voltage between the gate and source (negative V_{gs}). Since the junction of a depletion mode JFET is reverse biased in normal operation, the input voltage V_{gs} can be relatively high. However, the supply voltage between the drain and source (V_{ds}) is usually relatively low.

Prior Art FIG. **1** shows a general schematic for an n-channel depletion mode JFET with $V_{gs}=V_{ds}=0$. The JFET has two opposed gate regions **10**, a drain **11** and source **12**. The drain **11** and source **12** are located in the n-doped region of the device and the gates **10** are p-doped. Two p-n junctions are present in the device, each having an associated depletion region **13**. A conductive channel region **14** is shown between the two depletion regions **13** associated with the p-n junctions.

In operation, the voltage variable width of the depletion regions **13** is used to control the effective cross-sectional area of the conductive channel region **14**. The application of a voltage V_{gs} between the gates **10** and source **12** will cause the conductive channel region **14** to vary in width, thereby controlling the resistance between the drain **11** and the source **12**. A reverse bias, (e.g., a negative V_{gs}), will cause the depletion regions **13** to expand, and at a sufficiently negative value cause the conductive channel **14** to "pinch off", thereby turning off the device.

The width of the depletion regions **13** and the conductive channel region **14** are determined by the width of the n-doped region and the dopant levels in the n-doped and p-doped regions. If the device shown in FIG. **1** were constructed with a narrow n-doped region, such that the two depletion regions **13** merged into a single continuous depletion region and the conductive channel region **14** had zero width, the result would be the device shown in FIG. **2**.

Enhancement mode, or "normally off" JFETs are characterized by a channel that is sufficiently narrow such that a depletion region at zero applied voltage extends across the entire width of the channel. Application of a forward bias reduces the width of the depletion region in the channel, thereby creating a conduction path in the channel. P-channel enhancement mode JFETs are turned on by the application of a negative V_{gs}, and n-channel enhancement mode JFETs are turned on by the application of a positive V_{gs}. The input voltage of an enhancement mode JFET is limited by the forward voltage of the p-n junction.

Prior Art FIG. **2** shows a general schematic of an n-channel enhancement mode JFET with $V_{gs}=V_{ds}=0$. The enhancement mode device is "normally off" since the conductive channel width is zero due to the extent of the two depletion regions **13**B. The application of a sufficient forward bias (e.g. positive V_{gs}) to the device of FIG. **2** will cause the depletion regions **13**B to contract, thereby opening a conductive channel.

Although the depletion mode and enhancement mode devices shown schematically in FIG. **1** and FIG. **2** are n-channel devices, depletion mode and enhancement mode devices could be constructed with a reversed doping scheme to provide p-channel devices.

Historically, JFETs have been designed and manufactured with a single gate lead or gate input. Although prior art JFET devices may have more than one gate region associated with control of a conductive channel between source and drain, the gate regions are connected to a common input.

As with other transistor types, the operating characteristics of a JFET may be represented by a family of I-V curves corresponding to a set of inputs, e.g., drain current (I_d) versus drain/source voltage (V_{ds}) for different values of gate voltage (V_{gs}).

The operational characteristics of a JFET are typically determined by the geometric relationship between the gate, source and drain elements, and the doping profile in the substrate in which the JFET is fabricated. Devices may be fabricated with a wide range of characteristics, but operating parameters of a given device are essentially fixed.

In contrast to JFETs, metal-oxide semiconductor field effect transistors (MOSFETs) have been fabricated with multiple gate inputs that enable the fundamental operating characteristics of the MOSFET to be adjusted. For example, a DC voltage may be applied to one gate of a dual-gate MOSFET to shift the threshold voltage, or on resistance, of the device, with the other gate receiving the signal input.

MOSFETs have been more widely used than JFETs, and the fabrication processes for MOSFETs have been relatively more advanced than those used for JFETs. However, the adoption of submicron processes for device fabrication and the resulting higher speeds, lower voltages, and greater current demands in integrated circuits has created new opportunities for the application of JFETs.

JFETs are capable of being driven by low voltages while maintaining excellent breakdown characteristics when compared to MOSFETs. Since there is no insulator associated with gate/drain and gate/source interfaces of a JFET (only a p-n junction), forward bias results in conduction at voltages that are very low compared to the reverse bias that the device is capable of withstanding. JFETs also have a much greater resistance to damage from electrostatic discharge (ESD) than MOSFETs.

An obstacle to the adoption of JFETs for use in logic and power devices is a lack of precise control over process, voltage and temperature variations of conventional JFETs.